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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/977,787	10/15/2001	Udo Hartmann	W&B-INF-860	3729

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LERNER AND GREENBERG, PA
P O BOX 2480
HOLLYWOOD, FL 33022-2480

EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/977,787	HARTMANN, UDO	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☒ Claim(s) *1 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/115/2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-13 are presented for examination.

Priority

The examiner acknowledges claim for priority of 10/13/2000.

Information Disclosure Statement

The examiner has considered the Information Disclosure included with the application.

Claim Objections

1. Claim 1 is objected to because of the following informalities: line 13 of the claim, "a number of test data items" is ambiguous, in that the examiner believes the reference is to the test data items of line 9. If the test data items of line 13 refers to the teat data items of line 9, then the examiner suggests that line 13 be changed to read, "a number of the test data items". Appropriate correction is required.

2. Claim 9 is objected to because of the following informalities: the claim should have each step indented. See 37 CFR 1.75 and MPEP § 608.01(m). The claim or claims must commence on a separate sheet (37 CFR 1.52(b)). Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. There may be plural indentations to further segregate

subcombinations or related steps. See 37 CFR 1.75 and MPEP 608.01(i)- (p).

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1 to 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lepejian et al., U.S. Patent No. 6085346, and in view of Kanchira et al., U.S. Patent No. 6691271.

As per Claim 1:

Lepejian et al. teaches a circuit for testing a data memory (FIG.3 100), comprising: a processing unit connected to the data memory (contents of FIG.3), said processing unit applying a first function (FIG.3 60) to a predetermined test pattern (FIG.4 12) for generating therefrom data items to be written to the data memory (FIG.3

103), said processing unit reading the data items from the data memory (FIG.3 104) and a number of the data items (FIG.3 103) is greater than a number of test pattern data items (FIG.3 11); and a test device (FIG.4 20) connected to and outputting to said processing unit function data items defining the first function (FIG.4 22) and the second function (FIG.3 60) for said processing unit; wherein the second function is a reciprocal function of the first function (column 5 lines 51-56). Lepejian however fails to teach applying a second function to the data items read from the data memory for generating therefrom test data items. In an analogous art, Kanchira et al. teaches encoding a test signal (FIG.8 A) from a pattern generator using a 1st function (FIG.8 7), applying the new pattern (FIG.8 2A) to the circuit, and then applying a 2nd function to the new pattern (reciprocal in this case) to arrive at the original signal (FIG.8 A and column 9 lines 35-49). And Kanchira et al. recites an advantage to be; a circuit that easily generates a predetermined signal value for comparison with a test value for a test result in an integrated circuit without heavy circuit overhead (column 1 lines 53-67 and column 2 lines 1-30). And one with ordinary skill in the art at the time of the invention, motivated as suggested by Kanchira et al., would combine the two references, and so the claim is rejected.

As per Claim 2:

The circuit of Claim 1 is further limited wherein the number of data items defining the 1st function (Kanchira et al. FIG.8 7), which is 2A in this case, is greater than the number of test data items generated (Kanchira et al. FIG.8 9), which is A. As the math

proves herein, this is the case in Kanchira et al. and is therefore taught by the reference. And in view of the motivation previously stated, this claim is rejected.

As per Claim 3:

The circuit according to claim 1, wherein a number of the data items generated from the test pattern (Lepejian et al. FIG.3 103) for writing to the data memory is greater than a number of the test data items forming the test pattern (FIG. 3 11). The reference of Lepejian et al. teaches this, and in view of the motivation previously stated, the claim is rejected.

As per Claim 4:

The circuit according to claim 1, which comprises a comparison device connected to said processing device (Lepejian et al., FIG.3 80) and configured to determine from the test data items produced by said processing device (FIG.3 103) from the stored data items read from the data memory (FIG.3 104) whether the data memory is faulty (FIG.3 19). The reference of Lepejian et al. teaches this, and in view of the motivation previously stated, the claim is rejected.

As per Claim 5:

The circuit according to claim 1, which comprises a buffer store connected between said processing unit and the data memory (Lepejian et al., FIG.4 50 and FIG.5 53), for intermediately storing the data items produced from the test pattern data item (Lepejian et al., FIG.3 11) and writing to the data memory. The reference of Lepejian et al. teaches this, and in view of the motivation previously stated, the claim is rejected.

As per Claim 6:

The circuit according to claim 1, which comprises a buffer store connected between said processing unit and the data memory (Lepejian et al., FIG.3 80 and FIG.7 84), for intermediately storing the data items read from the data memory (Lepejian et al., FIG.3 104) and forwarding the data items for processing in said processing unit (Lepejian et al., FIG.7 Q outputs). The reference of Lepejian et al. teaches this, and in view of the motivation previously stated, the claim is rejected.

As per Claim 7:

Claim 7 is a combination of each of the Claims 5 and 6 together, and since both of the previous claims were rejected in view of Lepejian et al., this claim is also rejected in view of the same art and motivation.

As per Claim 8:

The claim limits the circuit of Claim 1 to be an integrated circuit. Lepejian et al., in column 1 lines 5-8, and column 12 lines 4-18, also teaches the circuit to being an integrated circuit, and in view of the motivation for Claim 1 above, this claim is rejected.

As per Claim 9:

Lepejian et al. teaches a method for testing a data memory (FIG.3 100), comprising: receiving a predetermined test pattern data item (column 9 lines 26-33 and FIG.4 12)) applying a first function (FIG.3 60) to a predetermined test pattern (FIG.4 12) for generating therefrom data items to be written to the data memory (FIG.3 103) which are a greater data width than the test pattern (FIG.4 12 > FIG.3 103), reading the data items from the data memory (FIG.3 104) and a test device (FIG.4 20) connected to and determining the first function (FIG.4 22) and the second function (FIG.3 60) for said

processing unit, wherein the second function is a reciprocal function of the first function (column 5 lines 51-56), and checking functionality of the memory (FIG.3 60 and 19). Lepejian however fails to teach applying a second function to the data items read from the data memory for generating test data items. In an analogous art, Kanchira et al. teaches encoding a test signal (FIG.8 A) from a pattern generator using a 1st function (FIG.8 7), applying the new pattern (FIG.8 2A) to the circuit, and then applying a 2nd function to the new pattern (reciprocal in this case) to arrive at the original signal (FIG.8 A and column 9 lines 35-49). And Kanchira et al. recites an advantage to be; a circuit that easily generates a predetermined signal value for comparison with a test value for a test result in an integrated circuit without heavy circuit overhead (column 1 lines 53-67 and column 2 lines 1-30). And one with ordinary skill in the art at the time of the invention, motivated as suggested by Kanchira et al., would combine the two references, and so the claim is rejected.

As per Claim 10:

The method according to claim 9, which comprises comparing a plurality of the test data items (Lepejian et al., FIG.3 103) with one another (Lepejian et al., FIG.3 104) in order to detect any fault in the data memory (Lepejian et al., FIG.3 19). The reference of Lepejian et al. teaches this, and in view of the motivation previously stated, the claim is rejected.

As per Claim 11:

The method according to claim 9, which comprises using the predetermined test pattern data item (Lepejian et al., FIG.3 11) as a stored data item (Lepejian et al., FIG.3

103) for the data memory. The reference of Lepejian et al. teaches this, and in view of the motivation previously stated, the claim is rejected.

As per Claim 12:

The method according to claim 9, which comprises storing the data items at one address in the data memory. As per FIG.3, for each address clock 13, one address in data memory 100 is applied to a write operation (column 6 lines 59-61), and in view of the motivation previously stated, the claim is rejected.

As per Claim 13:

The method according to claim 9, which comprises reading the stored data items from one address in the data memory. As per FIG.3, for each address clock 13, one address in data memory 100 is applied to a read operation (column 6 lines 59-61), and in view of the motivation previously stated, the claim is rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on weekdays, 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

jpt

Guy J. Lamarre
for
Albert DeCady
Primary Examiner